# Keyboard Encoder Circuits

For additional application information, see
AN-128 and AN-139 at the end of this section.

*NOT D.B.*

*not in D/B*

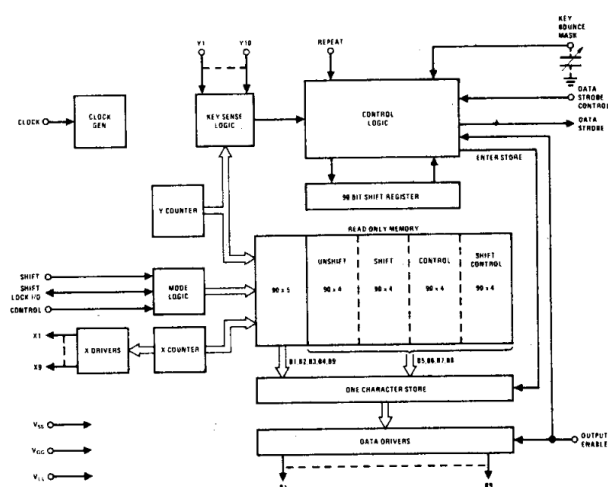## MM5740 90-key keyboard encoder

### general description

The MM5740 MOS/LSI keyboard encoder is a complete keyboard interface system capable of encoding 90 single pole single throw switch closures into a usable 9-bit code. It is organized as a bit paired system and is capable of N key or two key rollover. The MM5740 is fabricated with silicon gate technology and provides for direct TTL/DTL compatibility on Data and Strobe outputs without the use of any special interface components.
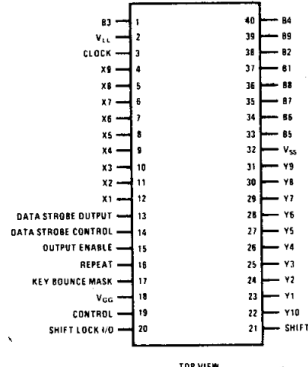
### features

- TRI-STATE® data outputs directly compatible with TTL/DTL or MOS logic

- Function inputs directly compatible with TTL/DTL logic

- Only one TTL level clock required

- N key/two key rollover (mask programmable)

- 90 key-quad mode capability

- One character data storage

- Repeat function (selectable)

- Shift lock with indicator capability

- Key bounce masking by single external capacitor

- Level or pulse data strobe output

- Data strobe pulse width control

## block and connection diagrams



**Dual-In-Line Package**

| | | | |
|---|---|---|---|
| B3 | 1 | 40 | B4 |
| V_LL | 2 | 39 | B9 |
| CLOCK | 3 | 38 | B2 |
| X9 | 4 | 37 | B1 |
| X8 | 5 | 36 | B8 |
| X7 | 6 | 35 | B7 |
| X6 | 7 | 34 | B6 |
| X5 | 8 | 33 | B5 |
| X4 | 9 | 32 | V_SS |
| X3 | 10 | 31 | Y9 |
| X2 | 11 | 30 | Y8 |
| X1 | 12 | 29 | Y7 |
| DATA STROBE OUTPUT | 13 | 28 | Y6 |
| DATA STROBE CONTROL | 14 | 27 | Y5 |
| OUTPUT ENABLE | 15 | 26 | Y4 |
| REPEAT | 16 | 25 | Y3 |
| KEY BOUNCE MASK | 17 | 24 | Y2 |
| V_GG | 18 | 23 | Y1 |
| CONTROL | 19 | 22 | Y10 |
| SHIFT LOCK I/O | 20 | 21 | SHIFT |

TOP VIEW

**Order Number MM5740N**
**See Package 24**

TRI-STATE is a registered trademark of National Semiconductor Corp.

# absolute maximum ratings

Data and Clock Input Voltages and Supply
   Voltages with Respect to $V_{SS}$          +0.3V to -20V
Power Dissipation               600 mW at $T_A = +25°C$
Operating Temperature         -25°C to +70°C ambient
Storage Temperature          -65°C to +160°C
Lead Temperature (Soldering, 10 seconds)         300°C

# electrical characteristics (Note 1,5)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Clock Repetition Rate | | 10 | | 200 | kHz |
| Clock Pulse Width | Rep. Rate = 200 kHz | 2.4 | | 2.6 | $\mu s$ |
| | Rep. Rate = 10 kHz | 20 | | 80 | $\mu s$ |
| Clock Amplitude | | | | | |
|   Logic Level "0" | | | | 3.25 | V |
|   Logic Level "1" | | +0.4 | | | V |
| Clock Transition Times | | | | | |
|   Risetime | Rep. Rate = 200 kHz | | | 100 | ns |
|   Falltime | Rep. Rate = 200 kHz | | | 100 | ns |
| Clock Input Capacitance | | | 5.0 | | pF |
| Data Input Levels, Y1 thru Y10 | | | | | |
|   Logic Level "0" | | | | $V_{SS} - 1.5$ | V |
|   Logic Level "1" | | -4.5 | | | V |
|   Logic Level "0" | | | | 3.25 | V |
|   Logic Level "1" | | +0.4 | | | V |
| Data Strobe Control | | | | | |
|   Logic Level "0" | | | | +3.5 | V |
|   Logic Level "1" | | +0.4 | | | V |
| Data Output Levels, X1 thru X9 | | | | | |
|   Logic Level "0" | When Connected to Y1 thru Y10 | | | $V_{SS} - 0.75$ | V |
|   Logic Level "1" | via Switch Matrix, ($C_L = 75$ pF) | -4.5 | | | V |
| B1 thru B9 and Data Strobe | | | | | |
|   Logic Level "0" | I = 100$\mu$A (Note 2) | | | $V_{SS} - 1.0$ | V |
|   Logic Level "1" | I = 1.6 mA (Note 2) | +0.4 | | | V |
| Shift Lock Voltage Open | Before Closure | | $V_{GG} + 2.0$ | | V |
| Shift Lock Voltage Closed | Switch Closed | | $V_{SS}$ | | V |
| Shift Lock Voltage Locked | After Release, (I = 1.0 mA) (Figure 2) | $V_{SS} - 5.0$ | | $V_{SS} - 8.0$ | V |
| Transition Times | | | | | |
|   Data Strobe ($T_{DS1}$) | $C_L = 100$ pF, I = 1.6 mA | | | 2.5 | $\mu s$ |
|   Data Strobe ($T_{DS0}$) | $C_L = 100$ pF, I = 100$\mu$A | | | 1.0 | $\mu s$ |
| Data Output Levels | | | | | |
|   ($T_{DO1}$) | $C_L = 100$ pF, I = 1.6 mA | | | 2.5 | $\mu s$ |
|   ($T_{DO0}$) | $C_L = 100$ pF, I = 100$\mu$A | | | 1.0 | $\mu s$ |
| Output Enable Setup Time ($T_{OES}$) | | 2.5 | | | $\mu s$ |
| Output Enable Release Time ($T_{OER}$) | | 2.5 | | | $\mu s$ |
| Repeat Input Pulse Width ($T_{RPW}$) | (Note 3) | | | | |
| | $f_{CLOCK} = 10$ kHz | 10 | | | ms |
| | $f_{CLOCK} = 200$ kHz | 0.5 | | | ms |
| Power Supply Current | $I_{GG}, I_{SS}$ | | 20 | 35 | mA |

**Note 1:** These specifications apply for $V_{SS} = +5.0$ VDC ±5%, $V_{GG} = -12.0$ VDC ±5%, $V_{LL}$ = GND and $T_A = 0°C$ to +70°C.

**Note 2:** When outputs B1 thru B9 and Data Strobe are driving TTL/DTL $V_{SS} - V_{LL} \leq 5.25$V. When driving MOS, $V_{SS} - V_{LL} \leq 10.0$V.

**Note 3:** Trpw min. = $100 \times \dfrac{1}{f\,clock}$

**Note 4:** If shift and control inputs are derived from a single pole, single throw switch closure to $V_{SS}$, a 100 OHM resistor returned to $V_{LL}$ (GND) is required on these inputs.

Note 5: The following inputs have internal pull-up resistors to $V_{SS}$: clock, output enable, repeat, shift, control.

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## description of pin functions

| NAME | PIN NO. | FUNCTION |
|------|---------|----------|
| X1-X9 | 4-12 | These pins are chip outputs which are used to drive the key switch matrix. When activated (at the appropriate scan time) they are driven high. |
| Y1-Y10 | 22-31 | Pins 22-31 are the Y sense inputs which are connected to the X drive lines via the key switch matrix. They are internally precharged to a low state and are pulled high upon switch closure. |
| B1-B9 | 1, 33-40 | These are the data outputs which represent the code for each keyswitch. They are TRI-STATE outputs with direct TTL compatibility. When the output enable input (Pin 15) is high, these outputs are in the third state. |
| Data Strobe Output | 13 | The function of this pin is to indicate that valid data has been entered by the keyboard and is ready for acceptance. An active data strobe is indicated by a high level. The data strobe may be operated in the pulse or level mode as indicated by the timing diagram. |
| Data Strobe Control | 14 | The basic purpose of this input is to provide data strobe output pulse width control. When connected to the data strobe output (Pin 13), the data strobe will exhibit a one bit wide pulse width. The pulse width may be varied by interposing an RC network between the data strobe output and the strobe control input. For level mode of operation the data strobe control input may be tied to $V_{SS}$ or to the data strobe output. |
| Output Enable | 15 | This input serves to TRI-STATE the data output (B1-B9) lines. In addition, it controls the return of the data strobe to the idle condition (low state) which is needed in the level strobe mode of operation. |
| Repeat | 16 | The repeat input is designed to accept a repeat signal via the repeat key. One data strobe will be issued for each positive interval of the repeat signal. Thus, if a 10 Hz signal is applied to the repeat input via the repeat switch, a 10 character per second data strobe will be issued when a data key and the repeat key are held depressed. |
| Key-Bounce Mask | 17 | This pin is intended as a timing node to mask switch key-bounce. The mask time interval is generated by connecting a capacitor to this pin. |
| Shift | 21 | When this input is brought to a logic "0" ($V_{SS}$) level, the encoder will assume the shifted character mode. |
| Control | 19 | A logic "0" places the encoder in the control character mode. |
| Shift Lock I/O | 20 | This pin is intended to serve as an input when the shift lock key is depressed. It places the encoder in the shift mode. Upon release of the key, the |

shift mode will be maintained and this pin will serve as an output to drive an indicator. This function is reset by depressing the shift key.

| | | | |
|---|---|---|
| Clock | 3 | A TTL compatible clock signal is applied to this pin. A bit time is defined as the time from one negative going transition to the succeeding negative going transition of the clock. |
| $V_{SS}$ | 32 | +5.0V supply |
| $V_{LL}$ | 2 | Ground |
| $V_{GG}$ | 18 | −12V supply |

10-4

## timing diagram
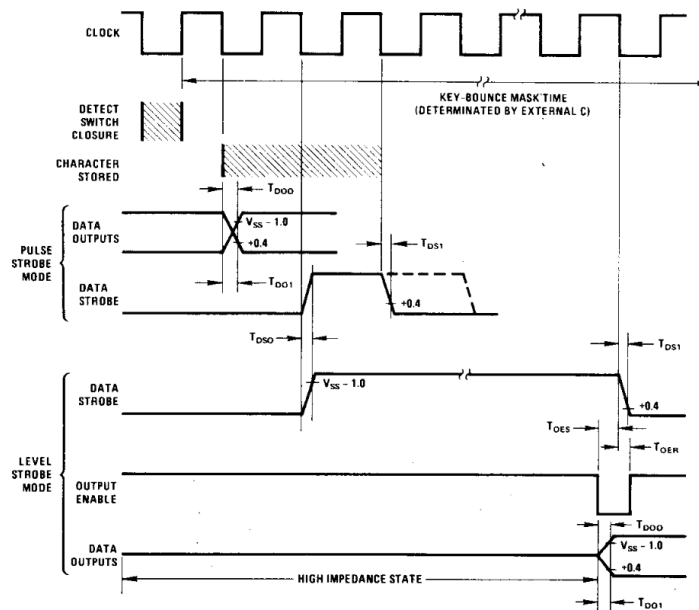


## applications information
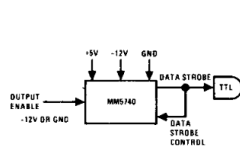


| A) DATA STROBE PULSE WIDTH = ONE CLOCK PERIOD | B) WIDER DATA STROBE PULSE WIDTH CONTROLLED BY RC | |
|---|---|---|
| **Pulse Data Strobe Mode** | | **Level Data Strobe Mode** |
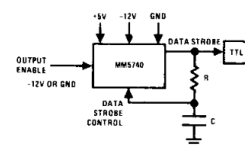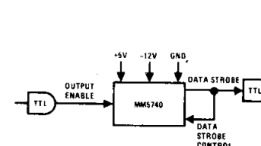
## key bounce capacitor values
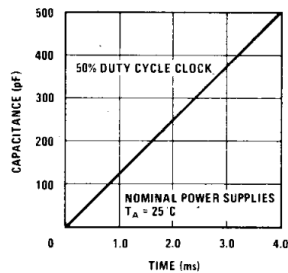
FIGURE 1. Key-Bounce Mask Time

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**MM5740**

## application
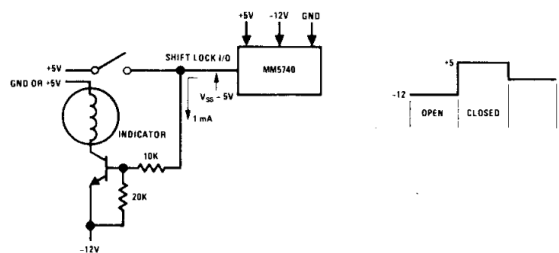


FIGURE 2. Shift Logic I/O Interface

## repeat switch function
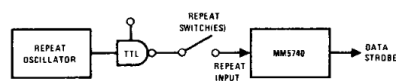


**Repeat Switch Connections**
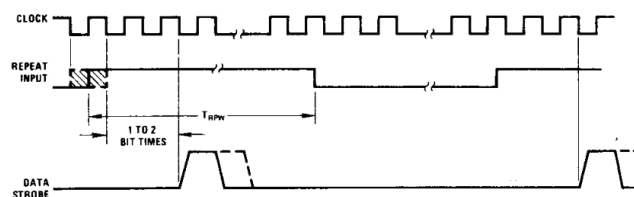


**Note:** Both Repeat Switch and a Data Key must be depressed to enable repeat function. For N-Key Rollover, the data outputs will represent the current valid data key (N Key Roll during Repeat).

# typical applications

GND
SHIFT KEY
CONTROL KEY
TTL TTL
+5V
CONTROL
100
SHIFT CONTROL
SHIFT LOCK
+5V
SHIFT LOCK INDICATOR
-12V

INSERT DIODES FOR N KEY ROLLOVER
KEY SWITCH MATRIX (90 MAX)
SINGLE POLE, SINGLE THROW, MOMENTARY

$V_{GG}$ -12V
$V_{SS}$ -5V
$V_{LL}$ GND

$X_1$ $X_0$ $Y_1$ $Y_{10}$

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REPEAT TTL
TTL CLOCK
TTL REPEAT CLOCK
KEY BOUNCE MASK

$B_1$ $B_4$
DATA STROBE CONTROL
DATA STROBE

TTL OUTPUT ENABLE

TTL TTL TTL

10-6

| | | COMMON | | | | | UNSHIFT | | | | SHIFT | | | | CONTROL | | | | SHIFT CONTROL | | | | CHARACTER | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **MATRIX ADDRESS** | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | Y | $B_1$ | $B_2$ | $B_3$ | $B_4$ | $B_9$ | $B_5$ | $B_6$ | $B_7$ | $B_8$ | $B_5$ | $B_6$ | $B_7$ | $B_8$ | $B_5$ | $B_6$ | $B_7$ | $B_8$ | $B_5$ | $B_6$ | $B_7$ | $B_8$ | US | S | C | SC |
| (Note 3) | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 7 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 9 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 5 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | |

CODE ASSIGNMENT CHART

Customer: _____

Date: _____

| | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | | | | | | | | | | | | | | | | | | | | | | |
| 8 | | | | | | | | | | | | | | | | | | | | | | |
| 9 | | | | | | | | | | | | | | | | | | | | | | |
| 10 | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | | |
| 2 | | | | | | | | | | | | | | | | | | | | | | |
| 3 | | | | | | | | | | | | | | | | | | | | | | |
| 4 | | | | | | | | | | | | | | | | | | | | | | |
| 5 | | | | | | | | | | | | | | | | | | | | | | |
| 6 | | | | | | | | | | | | | | | | | | | | | | |
| 7 | | | | | | | | | | | | | | | | | | | | | | |
| 8 | | | | | | | | | | | | | | | | | | | | | | |
| 9 | | | | | | | | | | | | | | | | | | | | | | |
| 10 | | | | | | | | | | | | | | | | | | | | | | |

☐ N-Key Rollover
☐ 2 Key Rollover
Page ☐ of 3 (Note 1)
Note: Use B8 if parity bit is desired

**Note 1:** 3 code assignment charts are required for each keyboard encoder pattern. Fill in a "1" or "0" in each output box ($B_1$ thru $B_9$). Indicate page number.

**Note 2:** The matrix is 9 "X" locations by 10 "Y" locations.

**Note 3:** Write in 10 one's, 10 two's, etc. in successive X address locations up to 9. This will fill 3 charts. The first page will have address matrix location 1,1; 1,2: 1,3... 1,10; 2,1; 2,2... 2,10; 3,1; etc. up to 3,10. Page 2 has 4,1 to 6,10. Page 3 has 7,1 to 9,10.

**Note 4:** A contact closure at the address matrix location will cause the appropriate bit pattern to appear at the output in negative true logic. $V_{OH}$ = "0"; $V_{OL}$ = "1."

**Note 5:** See application note AN-80 for coding example.

## MM5740

### MM5740AAE, MM5740AAF CODE ASSIGNMENT CHARTS

| MATRIX ADDRESS | | COMMON | | | | | UNSHIFT | | | | SHIFT | | | | CONTROL | | | | SHIFT CONTROL | | | | CHARACTER | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | Y | $B_1$ | $B_2$ | $B_3$ | $B_4$ | $B_9$ | $B_5$ | $B_6$ | $B_7$ | $B_8$ | $B_5$ | $B_6$ | $B_7$ | $B_8$ | $B_5$ | $B_6$ | $B_7$ | $B_8$ | $B_5$ | $B_6$ | $B_7$ | $B_8$ | US | S | C | SC |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 8 | 8 | 8 | 8 |
| 1 | 2 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 4 | 4 | 4 | 4 |
| 1 | 3 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 5 | 5 | 5 | 5 |
| 1 | 4 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 5 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 2 | 2 | 2 | 2 |
| 1 | 6 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 3 | 3 | 3 | 3 |
| 1 | 7 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | . | . | . | . |
| 1 | 8 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 6 | 6 | 6 | 6 |
| 1 | 9 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 9 | 9 | 9 | 9 |
| 1 | 10 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 7 | 7 | 7 | 7 |
| 2 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FF | FF | FF | FF |
| 2 | 2 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CR | CR | CR | CR |
| 2 | 3 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | FS | FS | FS | FS |
| 2 | 4 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | GS | GS | GS | GS |
| 2 | 5 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | VT | VT | VT | VT |
| 2 | 6 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | SO | SO | SO | SO |
| 2 | 7 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | SP | SP | SP | SP |

| X | Y | B1 | B2 | B3 | B4 | B9 | B5 | B6 | B7 | B8 | B5 | B6 | B7 | B8 | B5 | B6 | B7 | B8 | B5 | B6 | B7 | B8 | US | S | C | SC |
|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|----|
| 2 | 8 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HT | HT | HT | HT |
| 2 | 9 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | BS | BS | BS | BS |
| 2 | 10 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | | | | |
| 3 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | | | | |
| 3 | 2 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LF | LF | LF | LF |
| 3 | 3 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | P | | DLE | NUL |
| 3 | 4 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | DEL | DEL | DEL | DEL |
| 3 | 5 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | | | . | . |
| 3 | 6 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | | | . | . |
| 3 | 7 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | | | ? | ? |
| 3 | 8 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | P | P | DLE | DLE |
| 3 | 9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | O | O | SI | SI |
| 3 | 10 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | | | . | . |

| MATRIX ADDRESS | | COMMON | | | | | UNSHIFT | | | | SHIFT | | | | CONTROL | | | | SHIFT CONTROL | | | | CHARACTER | | | |
|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|----|
| X | Y | B1 | B2 | B3 | B4 | B9 | B5 | B6 | B7 | B8 | B5 | B6 | B7 | B8 | B5 | B6 | B7 | B8 | B5 | B6 | B7 | B8 | US | S | C | SC |
| 4 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | Q | 1 | Q | . |
| 4 | 2 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ! | ! | HT | HT |
| 4 | 3 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | O | | SI | US |
| 4 | 4 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | K | | VT | ESC |
| 4 | 5 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | L | | FF | FS |
| 4 | 6 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | | | | |
| 4 | 7 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | . | | . | . |
| 4 | 8 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | L | L | FF | FF |
| 4 | 9 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | K | K | VT | VT |
| 4 | 10 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 8 | ( | 8 | ( |
| 5 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 6 | & | G | & |
| 5 | 2 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | U | U | NAK | NAK |
| 5 | 3 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | Y | Y | EM | EM |
| 5 | 4 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | J | J | LF | LF |
| 5 | 5 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | H | H | BS | BS |
| 5 | 6 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | M | J | CR | GS |
| 5 | 7 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | N | | SO | RS |
| 5 | 8 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | M | M | CR | CR |
| 5 | 9 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | N | N | SO | SO |
| 5 | 10 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 7 | ' | 7 | ' |
| 6 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 5 | % | | |
| 6 | 2 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | R | R | DC2 | DC2 |
| 6 | 3 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | T | T | DC4 | DC4 |
| 6 | 4 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | F | F | ACK | ACK |
| 6 | 5 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | G | G | BEL | BEL |
| 6 | 6 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | V | V | SYN | SYN |
| 6 | 7 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | B | B | STX | STX |
| 6 | 8 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | CAN | CAN | CAN | CAN |
| 6 | 9 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | EM | EM | EM | EM |
| 6 | 10 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 4 | $ | 4 | $ |

Negative True Logic

$B_1 - B_7$ — ASCII Code

$\quad B_8$ = Even parity (on $B_1$, $B_2$, $B_3$, $B_4$, $B_5$, $B_6$, $B_7$, $B_8$)

$\quad B_9$ = Selective Repeat Bit

Note: Use $B_8$ if parity bit is desired.

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